DETAILED ACTION

Election/Restrictions

1. Claims 1 and 22 are allowable. The restriction requirement between groups I and II, as set forth in the Office action mailed on 7/11/08 has previously been withdrawn during the office action of 12/19/08.

2. The restriction requirement between groups A-C, as set forth in the Office action mailed on 8/25/09, has been reconsidered. Groups A-C were defined in terms of the claimed limitations as the claims existed on 8/25/09. Claims 10-20, directed to a non-elected species, have been canceled below by the examiner's amendment. The allowed claims 1-9 and 21-22, some of which originally belonged in elected group A, have been amended multiple times during prosecution between the restriction date and the date of this allowance notice. As such, the allowed invention is not accurately described by the features of group A that, on 8/25/09, had defined groups A-C and thus differentiated between groups A-C. Thus, there is an ambiguity as to how groups B and C would differ from the allowed invention. In order to remove any uncertainty, in the event that the applicant wishes to file a continuation application in the future, **the examiner hereby withdraws the restriction requirement between groups A-C as set forth on 8/25/09**.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present

application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Examiner's Amendment

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dan Vivarelli (Reg. No. 51137) on 10/18/11.

4. The application has been amended as follows (line numbers cited count fully deleted lines):

- In claim 1, at line 12, **delete** "pastes" and **insert** -- paste -- after "glass".
- In claim 1, at line 17, **delete** "pastes" and **insert** -- paste -- after "glass".
- In claim 3, at line 3, **delete** "premelting" and **insert** – pre-melting -- after "conditions and".
- In claim 3, at line 3, **delete** "premelting" and **insert** – pre-melting -- after "conditioning and the ".

- In claim 3, at line 4, **delete** "premelting" and **insert** – pre-melting -- after "conditioning and".
- In claim 5, at line 5, **delete** "joining" and **insert** -- bonding -- after "process of".
- In claim 21, at line 3, **delete** "side" after "surface".
- In claim 21, at line 5, **delete** "side" -- after "surface".
- In claim 21, at line 9, **insert** -- the -- after "layer of".
- In claim 21, at line 13, **insert** -- the -- after "layer of".
- **CANCEL** claims 11-19.

Allowable Subject Matter

5. Claims 1-9 and 21-22 are allowed. The following is an examiner's statement of reasons for allowance:

The prior art does not teach or suggest a process having all of the limitations of **claim 1**, including: providing patterned layers of the electrically non-conducting glass paste and the electrically conducting glass paste on said wafer surfaces, wherein the wafers are processed semiconductor wafers having electrically active structures thereon, and thereafter conditioning and pre-melting the electrically non-conducting glass paste and the electrically conducting glass paste, and thereafter bonding the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the

electrically conducting glass paste using a mechanical pressure. **Claims 2-9 and 21** depend from claim 1 and are allowable for the same reasons.

The prior art does not teach or suggest a process having all of the limitations of **claim 22**, including: providing a patterned layer of the electrically non-conducting glass paste on said wafer surfaces, wherein the wafers are processed semiconductor wafers having electrically active structures thereon, and applying a patterned layer of the electrically conducting glass paste on said wafer surfaces, and thereafter conditioning and pre-melting the electrically non-conducting glass paste and the electrically conducting glass paste, and thereafter bonding the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the electrically conducting glass paste using a mechanical pressure.

The closest prior art were discussed in the previous office actions. See the 6/10/11 office action. Warren, Ristic, and Kado were used in a 103 rejection. However, none of Warren, Ristic, and/or Kado teaches or suggests the claimed invention, including the processed semiconductor wafers having electrically active structures thereon. Rather, Warren teaches a core substrate made from a ceramic tape. Thus, ceramics are not semiconductor wafers, which are slabs of single-crystal semiconductor materials. In Warren, the active devices thus exist within the ceramic substrates, in depressions built into the substrate as seen in Fig. 2, not "thereon". The other prior art does not suggest the use of two processed semiconductor wafers instead of these ceramic substrates. Ristic has a semiconductor substrate 12 on one side but a cap 16

on the other side. The cap is formed of the same semiconductor material as is 12. However, it is not a processed wafer with an electrical device thereon. The references also do not suggest applying the patterned layers, and thereafter conditioning and pre-melting, and thereafter providing geometrical alignment, and thereafter bonding. As previously argued in the office action, the mixing of the glass frit and solvent in Ristic can be considered conditioning and Warren's mixing in the silver adhesive can be interpreted as conditioning. However, the examiner now notes that there is no suggestion to do these after applying patterned layers on the wafer surfaces.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments with respect to the pending claims have been considered.

7. The applicant argues that the 112 rejection should be withdrawn (pages 9 – top paragraph of page 11). The examiner agrees with the applicant that the "conditioning" must be done prior to applying the glass pastes to the wafer surfaces, according to the claimed language. Thus, the examples that the examiner gave in the rejection are not applicable. The examiner thus accepts the applicant's statements that the "FERRO" reference would tend to show that one of ordinary skill in the art would understand what "conditioning" is in terms of the glass pastes. The rejection is thus withdrawn.

The applicant argues that the 103 rejections should be withdrawn (page 12, first full paragraph – page 16 paragraph 3). The examiner agrees that the rejections should be withdrawn. The applicant has amended the independent claims to emphasize that the electrically active structures are in a central area of a stack of wafers; they emphasize in the arguments that the wafers are "processed semiconductor wafers having electrically active structures thereon". As discussed above, none of Warren, Ristic, and/or Kado teaches or suggests the claimed invention, including the processed semiconductor wafers having electrically active structures thereon. Rather, Warren teaches a core substrate made from a ceramic tape. Thus, ceramics are not semiconductor wafers, which are slabs of single-crystal semiconductor materials. In Warren, the active devices thus exist within the ceramic substrates, in depressions built into the substrate as seen in Fig. 2, not "thereon". The other prior art does not suggest the use of two processed semiconductor wafers instead of these ceramic substrates. Ristic has a semiconductor substrate 12 on one side but a cap 16 on the other side. The cap is formed of the same semiconductor material as is 12. However, it is not a processed wafer with an electrical device thereon. The references also do not suggest applying the patterned layers, and thereafter conditioning and pre-melting, and thereafter providing geometrical alignment, and thereafter bonding. As previously argued in the office action, the mixing of the glass frit and solvent in Ristic can be considered conditioning and Warren's mixing in the silver adhesive can be interpreted as conditioning. However, the examiner now notes that there is no suggestion to do these after applying patterned layers on the wafer surfaces. For these reasons, the 103

rejections are withdrawn. The applicant argues about claim 9 (page 16-17), and this is found allowable for the same reasons as claim 1, above.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Parendo, whose can be contacted by phone at (571) 270-5030 or directly by fax at (571) 270-6030. The examiner can normally be reached on Mon.-Thurs. and alternate Fridays from 7 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin A. Parendo/
Primary Examiner, Art Unit 2823
10/26/2011